IN THE CLAIMS

1. - 43. (Previously Canceled)

44. (Currently Amended) An integrated circuit comprising:

a layer of a titanium alloy covering the walls and bottom of a contact hole, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, ~~silicon,~~ germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the layer.

45. (Original) The integrated circuit of claim 34, wherein the titanium alloy comprises titanium and zinc.

46. - 59. (Previously Canceled)

60. (Currently Amended) An integrated circuit comprising:

a semiconductor substrate;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy covering the walls and bottom of a contact opening in the insulating layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, ~~silicon,~~ germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

61. (Previously Added) The integrated circuit of claim 60, wherein the titanium alloy includes titanium and zinc.

62. (Previously Added) The integrated circuit of claim 60, wherein the insulator layer includes silicon dioxide (SiO2).

63. (Previously Added) The integrated circuit of claim 60, wherein the electronic device includes a transistor.

64. (Currently Amended) An integrated circuit comprising:

a semiconductor substrate;

a transistor formed on the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy covering the walls and bottom of a contact opening in the insulating layer, the contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, ~~silicon,~~ germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

65. (Previously Added) The integrated circuit of claim 64, wherein the titanium alloy includes titanium and zinc.

66. (Previously Added) The integrated circuit of claim 64, wherein the insulator layer includes silicon dioxide (SiO2).

67. (Previously Added) The integrated circuit of claim 64, wherein the contact opening includes a high aspect ratio contact opening.

68. (Currently Amended) An integrated circuit comprising:

a semiconductor substrate;

an electronic device formed on the semiconductor substrate, the electronic device having an active region;

a borophosphous silicate glass (BPSG) layer over the active region;

an alloy layer of a titanium alloy covering the walls and bottom of a contact opening in the borophosphous silicate glass (BPSG) layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, ~~silicon,~~ germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

69. (Previously Added) The integrated circuit of claim 68, wherein the titanium alloy includes titanium and zinc.

70. (Previously Added) The integrated circuit of claim 68, wherein the electronic device includes a transistor.

71. (Previously Added) The integrated circuit of claim 68, wherein the contact opening includes a high aspect ratio contact opening.

72. (Currently Amended) An integrated circuit comprising:

a semiconductor substrate;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy covering the walls and bottom of a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element

selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, ~~silicon,~~ germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

73. (Previously Added) The integrated circuit of claim 72, wherein the titanium alloy includes titanium and zinc.

74. (Previously Added) The integrated circuit of claim 72, wherein the electronic device includes a transistor.

75. (Previously Added) The integrated circuit of claim 72, wherein the insulator layer includes silicon dioxide (SiO2).

76. (Previously Added) The integrated circuit of claim 72, wherein the insulator layer includes borophosphous silicate glass (BPSG).

77. (Currently Amended) An integrated circuit comprising:

a semiconductor substrate;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy covering the walls and bottom of a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, ~~silicon,~~ germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

78. (Previously Added) The integrated circuit of claim 77, wherein the titanium alloy includes titanium and zinc.

79. (Previously Added) The integrated circuit of claim 77, wherein the insulator layer includes silicon dioxide (SiO2).

80. (Previously Added) The integrated circuit of claim 77, wherein the insulator layer includes borophosphous silicate glass (BPSG).

81. (Currently Amended) An integrated circuit comprising:

a semiconductor substrate;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

a borophosphous silicate glass (BPSG) layer over the source/drain region;

an alloy layer of a titanium alloy covering the walls and bottom of a high aspect ratio contact opening in the borophosphous silicate glass (BPSG) layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, ~~silicon,~~ germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

82. (Previously Added) The integrated circuit of claim 81, wherein the titanium alloy includes titanium and zinc.

83. (Currently Amended) An integrated circuit comprising:

a semiconductor substrate;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy covering the walls and bottom of a contact opening in the insulating layer, the contact opening being at least partially over the active region, wherein the alloy layer is produced using a method including:

forming a seed layer supported by a substrate, wherein the seed layer is selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, germanium, lead, arsenic and antimony by combining a first precursor with a first reducing agent; and

forming the titanium alloy layer supported by the substrate by combining a titanium-containing precursor with the seed layer.